Abstracts

A 2-GHz RF front-end transceiver chipset in CMOS technology for PCS and IMT-2000 applications (2002 [RFIC])

Yong-Sik Youn, Nam-Soo Kim, Jae-Hong Chang, Young-Jae Lee and Hyun-Kyu Yu. "A 2-GHz RF front-end transceiver chipset in CMOS technology for PCS and IMT-2000 applications (2002 [RFIC])." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 271-274.

This paper describes RF front-end transceiver chipset for the dual-mode operation of PCS and IMT-2000. The transceiver chipset has been implemented in a 0.25 /spl mu/m single-poly five-metal CMOS technology. The receiver IC consists of a LNA and a down-mixer, and the transmitter IC integrates an up-mixer. Measurements show that the transceiver chipset covers the wide RF range from 1.8 GHz for PCS to 2.1 GHz for IMT-2000. The LNA has 2.5/spl sim/2.8 dB NF, 13/spl sim/12 dB gain and 6/spl sim/4 dBm IIP3. The down mixer has 15.5/spl sim/16.0 dB DSB NF, 15/spl sim/13 dB power conversion gain and 2/spl sim/0 dBm IIP3. The up mixer has 0/spl sim/-2 dB power conversion gain and 6/spl sim/3 dBm OIP3. With a single 3.0 V power supply, the LNA, down-mixer, and up-mixer consume 5 mA, 30 mA, and 25 mA, respectively.

❑ Return to main document.